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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,559	04/22/2004	Asher Hazanchuk	ALT.P030 (A1252)	6357

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/829,559	HAZANCHUK ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/22/04* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations/features cited in claims 1 and 7-8 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-20 cite a method and device for sum shift products in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-20 merely disclose steps/components for sum shift products without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 1-20 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for

patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 6-7, 9, and 11-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Regis (U.S. 6,907,024).

Re claim 1, Regis discloses in Figures 2, 4-5, and 8 a method for performing multiplication on a field programmable gate array (e.g. abstract and col. 1 lines 13-19 wherein the multiplication is performed in FIR filter; and general architecture is seen in Figure 4B), comprising:

generating a product (e.g. y_k as product of x inputs $[x_k - x_{k-3}]$ and c coefficients $[c_0 - c_3]$ in Figure 2 and as FIR 0 in Figure 4B) multiplying a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. the first number is x input and second number is the corresponding coefficient as simply seen in FIR Figure 2);

retrieving a stored value designated as a product (e.g. by utilizing LUTs as seen in Figure 8A or 8B) of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. the first number is x input and second number is the corresponding coefficient as simply seen in FIR 1 in Figure 4B);

scaling (e.g. by multiplying with corresponding weights 37 in Figure 4B) the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. multiplying w(0) 37 with product of FIR 0 as $y(0)_k$ by multiplier 24 in Figure 4B) and scaling (e.g. by multiplying with corresponding weights 37 in Figure 4B) the stored value with respect to

a position of the second plurality of bits from the second number and a position of the second plurality of bits from the second number(e.g. multiplying w(1) 37 with product of FIR 1 as $y(1)_k$ by multiplier 24 in Figure 4B); and

summing a scaled product and a scaled stored value (e.g. by adder 46 in Figure 4B).

Re claim 2, Regis further discloses in Figures 2, 4-5, and 8 generating the product comprises utilizing a digital signal processor (DSP) block (e.g. col. 1 lines 42-48).

Re claim 3, Regis further discloses in Figures 2, 4-5, and 8 the DSP block is configured to multiply two numbers of equal bit length (e.g. by four bits in length as seen in Figure 2 for each of FIR filter).

Re claim 4, Regis further discloses in Figures 2, 4-5, and 8 retrieving the stored value comprises utilizing a memory (e.g. Figures 8 with component 56 and corresponding table 1 in columns 6-7).

Re claim 6, Regis further discloses in Figures 2, 4-5, and 8 scaling the stored value comprises shifting bits in the product relative to a global least significant bit (e.g. Figures 4B and 8).

Re claim 7, Regis further discloses in Figures 2, 4-5, and 8 retrieving a second stored value designated as a product (e.g. FIR 2 in Figure 4B by using LUT technique as seen in Figure 8) of a third plurality of bits from the first number and a third plurality of bits from the second number (e.g. $x(2)_k$ and corresponding coefficients as seen generally in Figure 2); retrieving a third stored value designated as a product (e.g. FIR 3 in Figure 4B by using LUT technique as seen in Figure 8) of a fourth plurality of bits from the first

number and a fourth plurality of bits from the second number (e.g. $x(3)_k$ and corresponding coefficients as seen generally in Figure 2); scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number (e.g. by weight w(2) in Figure 4B) and scaling the third stored value with respect to a position of the fourth plurality of bits from the first number and a position of the fourth plurality of bits from the second number (e.g. by weight w(3) in Figure 4B); and summing a scaled second stored value and a scaled third stored value (e.g. by adder 46 in Figure 4B).

Re claim 9, it has similar limitations cited in claim 7. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 11, Regis discloses in Figures 2, 4-5, and 8 a method for implementing a multiplier on a field programmable gate array (e.g. abstract and col. 1 lines 13-19), comprising: configuring a digital signal processor (DSP) (e.g. col. 1 lines 42-48) to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. FIR 0 in Figure 4B with corresponding Figure 2); storing products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number in a memory (e.g. FIR 1 in Figure 4B with corresponding Figure 8B); routing an output from the DSP to an adder such that the output from the DSP is scaled according to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. scaling by input weights w(0) and w(1) in Figure 4B); routing an output of the memory to the adder such that the output from the memory is scaled according to a

position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. summing by adder 46 in Figure 4B).

Re claim 12, Regis further discloses in Figures 2, 4-5, and 8 storing products resulting from multiplication of a third plurality of bits from the first number and a third plurality of bits from the second number in a second memory (e.g. FIR 2 in Figure 4B with corresponding Figure 8B); storing products resulting from multiplication of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number in a third memory (e.g. FIR 3 in Figure 4B with corresponding Figure 8B); routing an output from the second memory to the adder such that the output from the second memory is scaled according to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number (e.g. scaling by weight w(2) in Figure 4B and final adder 46); and routing an output of the third memory to the adder such that the output from the memory is scaled according to a position of the fourth plurality of bits from the first number and a position of the fourth plurality of bits from the second number (e.g. scaling by weight w(3) in Figure 4B and final adder 46).

Re claim 13, Regis further discloses in Figures 2, 4-5, and 8 configuring the DSP comprises determining a number of bits that the DSP will multiply (e.g. col. 1 lines 42-48 and corresponding Figure 2).

Re claim 14, Regis further discloses in Figures 2, 4-5, and 8 determining a number of the second plurality of bits from the first number and a number of the second plurality of bits from the second number (e.g. Figure 2 as four-bits).

Re claim 15, Regis further discloses in Figures 2, 4-5, and 8 routing the output from the DSP has the effect of shifting the output from the DSP to a more significant bit position (e.g. Figures 2-3).

Re claim 16, Regis further discloses in Figures 2, 4-5, and 8 routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position (e.g. Figures 2-3 as FIR filter structural).

Re claim 17, Regis discloses in Figures 2, 4-5, and 8 a multiplier (e.g. Figure 4B) comprising a digital signal processor (DSP) (e.g. col. 1 lines 42-48) configured to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. by FIR 0 in Figure 4B with corresponding Figure 2); a memory that stores products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. by FIR 1 in Figure 4B with corresponding Figure 8B); and an adder that sums a scaled output of the DSP and a scaled output of the memory (e.g. scaling by weights w(0) and w(1) in Figure 4B and final adder 46).

Re claim 18, Regis further discloses in Figures 2, 4-5, and 8 the DSP, the memory, and the adder reside on a field programmable gate array (e.g. abstract and col. 2 lines 54-61).

Re claim 19, Regis further discloses in Figures 2, 4-5, and 8 a second memory that stores products resulting from multiplication of a third plurality of bits from the first number and a third plurality of bits from the second number (e.g. FIR 2 in Figure 4B with corresponding Figure 8B).

Re claim 20, Regis further discloses in Figures 2, 4-5, and 8 the adder sums a scaled output of the second memory with the scaled output of the DSP and the scaled output of the memory (e.g. final adder 46 in Figure 4B).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Regis (U.S. 6,907,024).

Re claim 5, Regis further discloses in Figures 2, 4-5, and 8 scaling the product relative to a global least significant bit (e.g. by multiplying with corresponding weights 37 in Figure 4B).

Regis fails to disclose the scaling by shifting bits in the product. However, multiplication by shifting is well-known in the art of technology and widely in many practical applications.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the shifting bit product as multiplication for scaling into Regis' invention because it would simplify the circuitry for performing multiplication.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 7,127,482 to Hou et al. disclose a performance optimized approach for efficient downsampling operations.

b. U.S. Patent No. 6,574,651 to Cui et al. disclose a method and apparatus for arithmetic operation on vectored data.

c. U.S. Patent No. 6,530,010 to Hung et al. disclose a multiplexer reconfigurable image processing peripheral having for loop control.

d. U.S. Patent No. 4,709,343 to Van Cang discloses a variable-passband and variable-phase digital filter.

e. U.S. Patent No. 6,425,070 to Zou et al. disclose a variable length instruction decoder.

f. U.S. Patent Publication No. 2005/0187997 to Zheng et al. disclose a flexible accumulator in digital signal processing circuitry.

g. U.S. Patent No. 6,014,684 to Hoffman discloses a method and apparatus for performing N bit by 2*N-1 bit signed multiplication.

h. U.S. Patent No. 6,907,024 to Regis discloses an efficient multichannel filtering for CDMA modems.

i. U.S. Patent No. 6,041,340 to Mintzer discloses a method for configuring an FPGA for large FFTs and other vector rotation computations.

j. U.S. Patent Publication No. 2004/0267857 to Abel et al. disclose a SIMD integer multiply high with round and shift.

k. U.S. Patent No. 7,003,542 to Devir discloses an apparatus and method for inverting a 4x4 matrix.

l. U.S. Patent No. 3,800,130 to Martinson et al. disclose a FFT stage using floating point numbers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

August 28, 2007